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# Scan Chain Stitching based on Logic Topology for Test-Power Reduction under Routing Constraint

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**ABSTRACT:** Scan architecture is a widely used design modification for testability in ASICs to obtain good test coverage. But during the process of scan testing, power consumption is much higher than in functional mode of operation, as all the flops in the design switch during scan shift operations (shift-in and shift-out). The heat generated from high power dissipation can destroy the chip, cause reliability problems, or induce noise. Sometimes the problem of wrong response due to overheating may arise, causing yield loss. For these reasons, test power reduction is a topic for research. Though there are several scan shift power optimization techniques used in practice, scan chain stitching techniques based on logic topology proposed in the recent years address both shift-in and shift-out powers. Conceptually, the techniques likely cause routing congestion and therefore applying the techniques under a routing constraint could be an optimal solution is the proposal presented in this paper.

**KEYWORDS:** Routing congestion, scan chain, Scan testing, shift-in and shift-out power, Test power.

## 1. INTRODUCTION

Test power is a concerning issue as it is much higher than the power consumption in functional mode. Designs with scan architecture are usually badly affected due to high test power. The scan shift power (shift-in and shift-out) is a major contributor to the test power. As all the flip flops in a design are stitched into a scan chain, and during the process of scan shift operations, all the flip flops undergo switching as the test vectors eventually enter the scan chain and shift through it, causing a high switching power consumption.
High test power is a concerning issue for the following reasons:

- Power consumption during scan testing is much higher than power during normal functional operation
- The heat generated from high power dissipation can destroy the chip, cause reliability problems, or induce noise
- Sometimes the problem of wrong response due to overheating may arise, causing yield loss

Several techniques have been proposed for test power reduction, scan chain stitching techniques based on logic topology address both scan shift-in and shift-out powers. The techniques described in [1, 2] are all dependent on test patterns. The scan flip flops are categorized as 0 dominant and 1 dominant based on the test vectors, similar scan flip flops are placed in adjacent part of scan chain so as to reduce the number of toggles and thereby reduce the test power. In order to optimize shift-in power, [3] describes a technique in which don't care dominant flip flops are to be stitched towards the end of the scan chain. The technique described in [4] is based on controllability measures. Controllability is a measure of the difficulty in setting a node to logic 0 or logic 1, represented as C0 and C1 respectively. When the difficulty in setting the input of a flip flop to 0 or 1 is known, we know how likely it is for the flip flop to capture a 0 or 1, thereby categorizing the flip flops into 0 dominant or 1 dominant is possible.

The technique described in [4] has been experimented on ISCAS'89 circuit and power optimization has been observed. Conceptually, the scan chain stitching techniques implemented without any PnR constraints cause routing congestion and therefore applying the techniques under a routing constraint could be an optimal solution is the proposal presented in this paper.

## 2. IMPLEMENTATION DETAILS

ISCAS'89 benchmark circuits have been used for the purpose. ISCAS'89 benchmark circuits are used for DFT researches as base for experiments. s27.v benchmark circuit has been chosen for the implementation.
All the flip flops in the circuit were replaced by scan flip flops, attaching 2x1 multiplexer to each of them to choose between functional mode and test mode. The scan flip flops were then stitched into a chain first in default method, i.e., in the alphabetical order of the instance names.

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The circuit was then simulated for scan testing – scan shift-in, capture, shift-out operations. In test mode, the scan chain functions as a shift register. The scan testing operation is done in three phases – Scan Shift-In, Scan Capture and Scan Shift-Out

In Scan Shift-In operation, Test Mode is selected in all the multiplexers. This will block the connections of the flip flops with the combinatorial cloud and configures the scan chain as a simple shift register. A test vector that was generated to detect a set of stuck at faults is applied through the SI pin serially shifting the bits at every clock cycle. Once the test vector has completely entered into the scan chain, Functional Mode is selected in all the multiplexers, and the clock cycle which followed by, captures the data from the combinational cloud, this phase is called Scan Capture. The data thus captured is then shifted out by switching back to Test Mode and configuring the scan chain as a shift register again, this serially shifted output is then compared to the expected output; if the actual response is same as the expected response, we conclude there are no stuck at faults which the test vector is meant to detect, otherwise we conclude there are stuck at faults.

Simulation results were as expected. A TCF (Toggle Count File) was generated to record the number of toggles with default scan chain stitching.

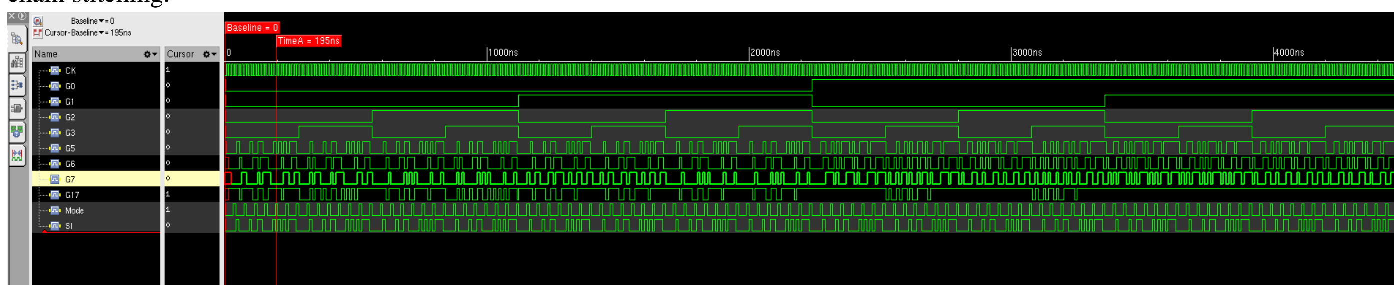


**Figure 1 -** Simulation results of scan shift-in, capture and shift-out operations

In order to optimize test power, scan chain stitching was done based on logic topology, i.e, based on the controllability values at the input pins of the flip flops. A C code was developed to evaluate the controllability values as per the SCOAP measures algorithm described in [5]. Scan chain stitching was done in the decreasing order of controllability values (C0) in order to reduce the number of toggles in scan shift operation.

Scan testing was then simulated and a TCF was generated to record the number of toggles with scan chain stitching based on logic topology.

## 3. EXPERIMENTAL RESULTS

The simulations for scan testing, TCF files generation, followed by synthesis to map to actual cells in the technology library were performed on Cadence Genus tool.

The Toggle count comparison for s27.v benchmark circuit is presented below

**Table 1 -** Toggle count comparison for s27.v benchmark circuit

| Port name | Port type | Toggle count Default Scan Chain | Toggle count LT based Scan Chain |
|---|---|---|---|
| G5 | out | 223 | 215 |
| G6 | out | 214 | 188 |
| G7 | out | 230 | 210 |
| G17 | out | 108 | 94 |
| SI | in | 224 | 224 |
| Mode | in | 223 | 223 |
| CK | in | 896 | 896 |
| G0 | in | 1 | 1 |
| G1 | in | 3 | 3 |
| G2 | in | 7 | 7 |
| G3 | in | 15 | 15 |

As can be noticed from the numbers in the table, the toggle counts on all input ports are same for both default scan chain design and logic topology-based scan chain design; whereas, on all the output ports and all flipflop output pins, the numbers of toggles have reduced in design with logic topology-based scan chain.

On synthesising and reporting power, the switching power was observed to have reduced by 4nW in the design with logic topology-based scan chain stitching.

| Category | Leakage | Internal | Switching | Total | Row% |
|---|---|---|---|---|---|
| memory | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| register | 3.54431e-10 | 9.68875e-07 | 9.67590e-08 | 1.06599e-06 | 95.84% |
| latch | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| logic | 1.23756e-10 | 2.95578e-08 | 1.65541e-08 | 4.62357e-08 | 4.16% |
| bbox | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| clock | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| pad | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| pm | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| Subtotal | 4.78187e-10 | 9.98433e-07 | 1.13313e-07 | 1.11222e-06 | 100.00% |

**Figure 2 –** Power metrics results for design with default scan chain stitching

| Category | Leakage | Internal | Switching | Total | Row% |
|---|---|---|---|---|---|
| memory | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| register | 3.53992e-10 | 9.38486e-07 | 9.51687e-08 | 1.03401e-06 | 96.26% |
| latch | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| logic | 1.24086e-10 | 2.55458e-08 | 1.44785e-08 | 4.01483e-08 | 3.74% |
| bbox | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| clock | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| pad | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| pm | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00000e+00 | 0.00% |
| Subtotal | 4.78078e-10 | 9.64032e-07 | 1.09647e-07 | 1.07416e-06 | 100.00% |

**Figure 3 -** Power metrics results for design with LT based scan chain stitching

As observed from the power metrics reported, there is ~4nW switching power reduction and ~38nW total power reduction in design with logic topology-based scan chain as compared to a design with default scan chain.

**Table 2 –** Power metrics comparison

| Power type | Default scan chain | LT based scan chain |
|---|---|---|
| Switching power | 113.3 nW | 109.6 nW |
| Internal power | 998.43 nW | 964.03 nW |
| Total power | 1112.2 nW | 1074.1 nW |

## 4. CONCLUSION

As expected, power optimisation has been observed using logic topology-based scan chain stitching, but on using the logic topology-based scan chain stitching technique there is every possibility of routing congestion in physical implementation.

As the placement of the standard cells happens considering factors in functional mode and the logic topology-based scan chain stitching technique stitches the flops based on their controllability numbers, there is every possibility of the flops with matching controllability numbers to be placed far away from each other which could cause routing congestion as shown in the figures below.

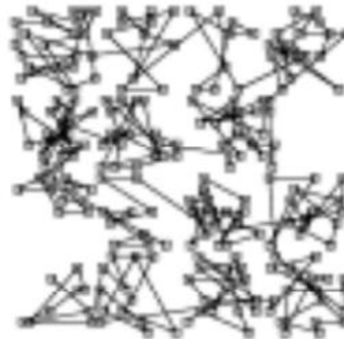

**Figure 4 -** Routing congestion without scan re-ordering

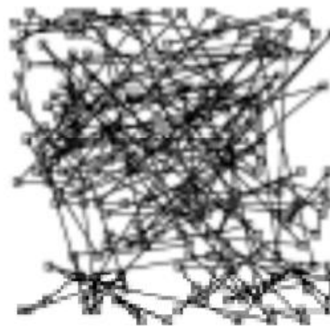

**Figure 5 -** Routing congestion with scan re-ordering

In order to avoid the routing congestion that could turn out to be a drawback of the logic topology-based scan chain stitching, we could add a routing constraint.

First a set of clusters for scan flip flops could be created using K means or modified K means algorithms based on the placement of the scan flip flops. Scan chain stitching should be confined to the scan flip flops belonging to the same cluster, this way routing congestion can be avoided with a little trade off with the test power.

After clustering the floorplan would look like below

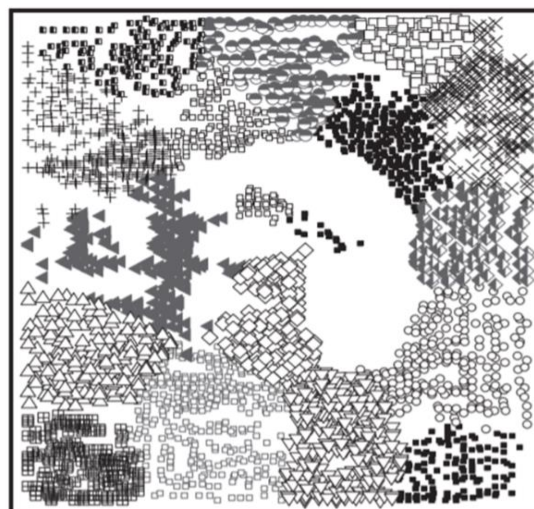

**Figure 6 -** Clustering scan flip flops based on K Means algorithm

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